AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

COMPLETE LISTING OF CLAIMS:

Claims 1-17 : (Canceled)

Claim 18 : (New) A method of controlling a bias voltage of an avalanche photodiode in an optical communications system including forward error correction, the method comprising the steps of:

a) measuring an error rate in an electrical signal converted from an optical signal by the avalanche photodiode over a plurality of sample periods; and

b) adjusting the bias voltage applied to the avalanche photodiode to minimize the error rate in the electrical signal by determining whether the error rate is increasing or decreasing with time.

Claim 19 : (New) The method according to claim 18, and determining the bias voltage by a value of a counter which is incremented or decremented every sample period, and changing a count direction of the counter if the error rate is increasing with time.

Claim 20 : (New) The method according to claim 19, and inhibiting movement of a clock if the error rate is zero.

Claim 21 : (New) The method according to claim 20, and determining the sample period by a clock tick of the clock.

Claim 22 : (New) The method according to claim 21, and varying an interval between clock ticks of the clock.

Claim 23 : (New) The method according to claim 22, wherein the interval between the clock ticks varies in dependence on the measured error rate.

Claim 24 : (New) The method according to claim 23, wherein there is a plurality of possible lengths of the interval, and selecting the interval of increased length if the error rate is below a first level, and of decreased length if the error rate is above a second level.

Claim 25 : (New) An apparatus for controlling a bias voltage of an avalanche photodiode (APD) in an optical communications system including forward error correction (FEC), comprising: an error rate measurer for measuring an error rate in an electrical signal converted from an optical signal by the APD; and an adjustment circuit for adjusting the bias voltage applied to the APD to minimize the error rate, the adjustment circuit comprising decision logic for determining whether the error rate is increasing or decreasing with time.

Claim 26 : (New) The apparatus according to claim 25, wherein the adjustment circuit comprises a counter, a counter value of which determines a level of the bias voltage, and means for changing a count direction of the counter if the decision logic determines that the error rate is increasing with time.

Claim 27 : (New) The apparatus according to claim 26, wherein the means for changing the count direction is a toggle.

Claim 28 : (New) The apparatus according to claim 27, comprising a digital to analog converter for converting the counter value to an analog APD bias voltage.

Claim 29 : (New) The apparatus according to claim 28, wherein the adjustment circuit comprises an error pulse counter for counting error pulses over a predetermined interval, and a store for holding error counts for a plurality of earlier intervals.

Claim 30 : (New) The apparatus according to claim 29, wherein the decision logic operates on the error counts held in the store.

Claim 31 : (New) The apparatus according to claim 30, comprising means for varying the interval over which error pulses are counted.

Claim 32 : (New) The apparatus according to claim 31, wherein the interval varying means varies the interval in dependence on the error rate.

Claim 33 : (New) The apparatus according to claim 32, wherein the interval varying means varies the interval between one of a plurality of different interval lengths.

Claim 34 : (New) The apparatus according to claim 26, comprising an inhibitor for inhibiting movement of the counter if the error rate is zero.